~~9425 October 9, 1997~~

US PAT NO: 5,629,637 [IMAGE AVAILABLE] L16: 1 of 3
TITLE: Method of time multiplexing a programmable logic device

US PAT NO: 5,600,263 [IMAGE AVAILABLE] L16: 2 of 3
TITLE: Configuration modes for a time multiplexed programmable logic device

US PAT NO: 5,583,450 [IMAGE AVAILABLE] L16: 3 of 3
TITLE: Sequencer for a time multiplexed programmable logic device

(FILE 'USPAT' ENTERED AT 12:42:55 ON 17 APR 1998)
SET HIGHLIGHT OFF

```
L1        1106 S (326/93 OR 326/94 OR 326/95 OR 326/96 OR 326/97 OR 326/9
8)/
L2        1615 S (711/100 OR 711/167 OR 711/168 OR 711/169)/CCLS OR L1
L3        1135 S L2 AND CLOCK?
L4         616 S L2 AND PHAS?
L5         923 S L2 AND MEMOR?
L6        1101 S L2 AND DATA?
L7         569 S L2 AND BUS?
L8         316 S L2 AND ERROR?
L9        1143 S L2 AND DIFFEREN?
L10       1300 S L2 AND CONTROL?
L11        607 S L2 AND SYNCHRON?
L12         46 S L3 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9 AND L10 AND
 L1
L13           6 S L12 AND PHAS? (5A) ERROR?
L14          13 S L12 AND PHAS? (P) DIFFEREN?
L15          24 S L12 AND CLOCK? (5A) PHAS?
L16           3 S L13 AND L14 AND L15
```

US PAT NO: 5,666,322 [IMAGE AVAILABLE] L14: 1 of 2
TITLE: Phase-locked loop timing controller in an integrated circuit memory

US PAT NO: 5,577,236 [IMAGE AVAILABLE] L14: 2 of 2
TITLE: Memory controller for reading data from synchronous RAM

(FILE 'USPAT' ENTERED AT 13:05:50 ON 17 APR 1998)
DELETE HISTORY Y

L1 13 SEARCH (5479646 OR 5550783 OR 5192914 OR 5692165 OR 485800
9 O
L2 13 SEARCH (5418924 OR 5646564 OR 5504752 OR 5274678 OR 565510
5 O
L3 13 SEARCH (4800534 OR 4641044 OR 5260909 OR 5208783 OR 540238
9 O
L4 11 SEARCH (5239639 OR 5479647 OR 4959814 OR 5416746 OR 557723
6 O
L5 50 SEARCH L1 OR L2 OR L3 OR L4
L6 9 S L5 AND PHAS? (5A) DIFFEREN?
L7 41 S L5 AND MEMOR? (5A) CONTROL?
L8 3 S L5 AND PHAS? (5A) ERROR?
L9 23 S L5 AND DATA? (5A) BUS?
L10 0 S L5 AND ECHO? (5A) CLOCK?
L11 10 S L5 AND PHAS? (5A) DELAY?
L12 43 S L5 AND DATA? (5A) CLOCK?
L13 11 S L6 OR L8
L14 2 S L7 AND L9 AND L11 AND L12 AND L13

~~9:25 October 9,~~ 1997

US PAT NO: 5,287,537 [IMAGE AVAILABLE] L40: 1 of 6
TITLE: Distributed processing system having plural computers each using identical retaining information to identify another computer for executing a received command

US PAT NO: 5,016,162 [IMAGE AVAILABLE] L40: 2 of 6
TITLE: Contention revolution in a digital computer system

US PAT NO: 4,933,846 [IMAGE AVAILABLE] L40: 3 of 6
TITLE: Network communications adapter with dual interleaved memory banks servicing multiple processors

US PAT NO: 4,920,483 [IMAGE AVAILABLE] L40: 4 of 6
TITLE: A computer memory for accessing any word-sized group of contiguous bits

US PAT NO: 4,443,850 [IMAGE AVAILABLE] L40: 5 of 6
TITLE: Interface circuit for subsystem controller

US PAT NO: 4,009,344 [IMAGE AVAILABLE] L40: 6 of 6
TITLE: Inter-related switching, activity compression and demand assignment

(FILE 'USPAT' ENTERED AT 17:03:16 ON 13 APR 1998)
SET HIGHLIGHT OFF

L1	0	S	(326 AND 370 AND 375 AND 395 AND 711)/CLAS
L2	66698	S	(326 OR 370 OR 375 OR 395 OR 711)/CLAS
L3	28728	S	L2 AND CLOCK?
L4	37611	S	L2 AND MEMOR?
L5	27412	S	L2 AND BUS?
L6	52207	S	L2 AND CONTROL?
L7	53630	S	L2 AND SIGN?
L8	9180	S	L2 AND MAST?
L9	20041	S	L2 AND PHAS?
L10	27573	S	L2 AND DELAY?
L11	2231	S	L2 AND ECHO?
L12	49432	S	L2 AND DATA?
L13	16506	S	L2 AND COMMAND
L14	7543	S	L2 AND PACKET?
L15	10613	S	L2 AND PROTOCOL?
L16	344	S	L2 AND PROPOGAT?
L17	54	S	L2 AND VERNIER?
L18	1776	S	L3 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9 AND L10
L19	0	S	L11 AND L12 AND L13 AND L14 AND L15 AND L16 AND L17
L20	2	S	L11 AND L12 AND L13 AND L14 AND L15 AND L16
L21	94	S	L11 AND L12 AND L13 AND L14 AND L15 AND L18
L22	1	S	L11 AND L12 AND L13 AND L14 AND L16 AND L18
L23	1	S	L11 AND L12 AND L13 AND L15 AND L16 AND L18
L24	1	S	L11 AND L12 AND L14 AND L15 AND L16 AND L18
L25	1	S	L11 AND L13 AND L14 AND L15 AND L16 AND L18
L26	4	S	L12 AND L13 AND L14 AND L15 AND L16 AND L18

L27	4	S	L22 OR L23 OR L24 OR L25 OR L26
L28	97	S	L[redacted] OR L22 OR L23 OR L24 OR L25 OR [redacted]6
L29	6	S	L28 AND PHAS? (6A) DELAY? (6A) CLOCK?
L30	74	S	L28 AND MEMOR? (3A) CONTROL?
L31	43	S	L28 AND CLOCK? (5A) BUS?
L32	16	S	L28 AND MEMOR? (5A) CLOCK?
L33	0	S	L29 AND L30 AND L31 AND L32
L34	5	S	L29 AND L30 AND L31
L35	1	S	L29 AND L30 AND L32
L36	0	S	L29 AND L31 AND L32
L37	10	S	L28 AND L31 AND L32
L38	12	S	L34 OR L35 OR L37 AND SYNCHRON? (5A) MEMOR?
L39	6	S	L38 AND MEMOR? (3A) CLOCK?
L40	6	S	L39 AND MEMOR? (3A) BUS?
L41	0	S	L40 AND ECHO? (3A) CLOCK?
L42	4	S	L38 AND ECHO? (3A) CLOCK?

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     (FILE 'USPAT' ENTERED AT 10:05:35 ON 15 APR 1998)
                SET HIGHLIGHT OFF
L1          1105 S (326/93 OR 326/94 OR 326/95 OR 326/96 OR 326/97 OR 326/9
8)/
L2          1614 S L1 OR (711/100 OR 711/167 OR 711/168 OR 711/169)/CCLS
L3          1135 S L2 AND CLOCK?
L4           923 S L2 AND MEMOR?
L5          1300 S L2 AND CONTROL?
L6           569 S L2 AND BUS?
L7          1437 S L2 AND SIGN?
L8           210 S L2 AND MAST?
L9           616 S L2 AND PHAS?
L10          892 S L2 AND DELAY?
L11            4 S L2 AND ECHO?
L12         1101 S L2 AND DATA?
L13          276 S L2 AND COMMAND?
L14           37 S L2 AND PACKET?
L15           91 S L2 AND PROTOCOL?
L16           15 S L2 AND PROPOGAT?
L17            0 S L2 AND VERNIER?
L18           38 S L3 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9 AND L10
L19            8 S L12 AND L13 AND L15 AND L18
L20            3 S L14 AND L19
L21            0 S L16 AND L19
L22           47 S L2 AND MULTIPROCESS?
L23            4 S L18 AND L22

=> d ti l20 1-3; d ti l23 1-4


US PAT NO:      5,687,081 [IMAGE AVAILABLE]            L20: 1 of 3
TITLE:          Lift truck control system

US PAT NO:      5,606,717 [IMAGE AVAILABLE]            L20: 2 of 3
TITLE:          Memory circuitry having bus interface for receiving
                  information in packets and access time registers

US PAT NO:      5,499,385 [IMAGE AVAILABLE]            L20: 3 of 3
TITLE:          Method for accessing and transmitting data to/from a
                  memory in packets



US PAT NO:      5,579,512 [IMAGE AVAILABLE]            L23: 1 of 4
TITLE:          Systempro emulation in a symmetric multiprocessing
                  computer system

US PAT NO:      5,522,069 [IMAGE AVAILABLE]            L23: 2 of 4
TITLE:          Symmetric multiprocessing system with unified environment
                  and distributed system functions

US PAT NO:      5,485,594 [IMAGE AVAILABLE]            L23: 3 of 4
TITLE:          Apparatus and method using an atomic fetch and add for
                  establishing temporary ownership of a common system
```

resource in a multiprocessor data processing system

US PAT NO: 4,390,970 [IMAGE AVAILABLE] L23: 4 of 4
TITLE: Rotating register utilizing field effect transistors

9:25 October 9, 1997

US PAT NO: 5,692,165 [IMAGE AVAILABLE] L9: 1 of 5
TITLE: **Memory controller** with low skew **control** signal

US PAT NO: 5,634,042 [IMAGE AVAILABLE] L9: 2 of 5
TITLE: Data transfer apparatus that compensates for differential signal delays

US PAT NO: 5,276,858 [IMAGE AVAILABLE] L9: 3 of 5
TITLE: **Memory controller** with integrated delay line circuitry

US PAT NO: 4,435,779 [IMAGE AVAILABLE] L9: 4 of 5
TITLE: Data processing system with programmable graphics generator

US PAT NO: 3,938,094 [IMAGE AVAILABLE] L9: 5 of 5
TITLE: Computing system bus

US PAT NO: 5,692,165 [IMAGE AVAILABLE] L10: 1 of 3
TITLE: **Memory controller** with low skew **control** signal

US PAT NO: 5,276,858 [IMAGE AVAILABLE] L10: 2 of 3
TITLE: **Memory controller** with integrated delay line circuitry

US PAT NO: 3,938,094 [IMAGE AVAILABLE] L10: 3 of 3
TITLE: Computing system bus

(FILE 'USPAT' ENTERED AT 10:05:35 ON 15 APR 1998)
SET HIGHLIGHT OFF
L1 1105 S (326/93 OR 326/94 OR 326/95 OR 326/96 OR 326/97 OR 326/98)/
L2 1614 S L1 OR (711/100 OR 711/167 OR 711/168 OR 711/169)/CCLS
L3 1135 S L2 AND CLOCK?
L4 923 S L2 AND MEMOR?
L5 86 S L2 AND PHAS? (5A) DELAY?
L6 440 S L2 AND MEMOR? (5A) CONTROL?
L7 275 S L2 AND MEMOR? (5A) BUS?
L8 134 S L2 AND CLOCK? (5A) BUS?
L9 5 S L5 AND L6 AND L7
L10 3 S L3 AND L8 AND L9

9:25 October 9, 1997

```
     (FILE 'USPAT' ENTERED AT 10:05:35 ON 15 APR 1998)
               SET HIGHLIGHT OFF
L1          1105 S (326/93 OR 326/94 OR 326/95 OR 326/96 OR 326/97 OR 326/9
8)/
L2          1614 S L1 OR (711/100 OR 711/167 OR 711/168 OR 711/169)/CCLS
L3          1135 S L2 AND CLOCK?
L4           923 S L2 AND MEMOR?
L5          1300 S L2 AND CONTROL?
L6           569 S L2 AND BUS?
L7          1437 S L2 AND SIGN?
L8           210 S L2 AND MAST?
L9           616 S L2 AND PHAS?
L10          892 S L2 AND DELAY?
L11            4 S L2 AND ECHO?
L12         1101 S L2 AND DATA?
L13          276 S L2 AND COMMAND?
L14           37 S L2 AND PACKET?
L15           91 S L2 AND PROTOCOL?
L16           15 S L2 AND PROPOGAT?
L17            0 S L2 AND VERNIER?
L18           38 S L3 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9 AND L10
L19            8 S L12 AND L13 AND L15 AND L18
L20            3 S L14 AND L19
L21            0 S L16 AND L19
L22           47 S L2 AND MULTIPROCESS?
L23            4 S L18 AND L22

=> d ti l20 1-3; d ti l23 1-4


US PAT NO:      5,687,081 [IMAGE AVAILABLE]            L20: 1 of 3
TITLE:          Lift truck control system

US PAT NO:      5,606,717 [IMAGE AVAILABLE]            L20: 2 of 3
TITLE:          Memory circuitry having bus interface for receiving
                  information in packets and access time registers

US PAT NO:      5,499,385 [IMAGE AVAILABLE]            L20: 3 of 3
TITLE:          Method for accessing and transmitting data to/from a
                  memory in packets



US PAT NO:      5,579,512 [IMAGE AVAILABLE]            L23: 1 of 4
TITLE:          Systempro emulation in a symmetric multiprocessing
                  computer system
```

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US PAT NO: 5,522,069 [IMAGE AVAILABLE] L23: 2 of 4
TITLE: Symmet[redacted] multiprocessing system with u[redacted]ed environment and distributed system functions

US PAT NO: 5,485,594 [IMAGE AVAILABLE] L23: 3 of 4
TITLE: Apparatus and method using an atomic fetch and add for establishing temporary ownership of a common system resource in a multiprocessor data processing system

US PAT NO: 4,390,970 [IMAGE AVAILABLE] L23: 4 of 4
TITLE: Rotating register utilizing field effect transistors

US PAT NO: 5,692,165 [IMAGE AVAILABLE] L19: 1 of 1
TITLE: **Memory controller** with low skew **control** signal

(FILE 'USPAT' ENTERED AT 16:10:59 ON 20 APR 1998)

```
L1          754 S DELAY? (6A) LOCK? (6A) LOOP?
L2            4 S L1 AND (395/551)/CCLS
L3            0 S L1 AND 711/162/CCLS
L4            2 S L2 AND MEMOR?
L5            4 S L2 AND CONTROL?
L6            4 S L2 AND CLOCK?
L7            4 S L2 AND DATA?
L8            2 S L2 AND BUS?
L9            4 S L2 AND PHAS?
L10           4 S L2 AND DELAY?
L11           0 S L2 AND ECHO?
L12           4 S L2 AND SYNCHRON?
L13           2 S L4 AND L5 AND L6 AND L7 AND L8 AND L9 AND L10 AND L12
L14           1 S L13 AND PHAS? (3A) DELAY?
L15           1 S L13 AND SYNCHRON? (3A) MEMOR?
L16           2 S L13 AND MEMOR? (3A) CLOCK?
L17           2 S L13 AND MEMOR? (3A) CONTROL?
L18           0 S L14 AND L15 AND L16 AND L17
L19           1 S L14 AND L16 AND L17
```

US PAT NO: 5,020,023 [IMAGE AVAILABLE] L2: 1 of 1
TITLE: Automatic vernier synchronization of skewed data streams

(FILE 'USPAT' ENTERED AT 14:02:53 ON 20 APR 1998)
SET HIGHLIGHT OFF
L1 3434 S VERNIER?
L2 1 S L1 AND (395/551 OR 395/405 OR 395/432 OR 395/494 OR 395/505
L3 0 S L1 AND 711/162/CCLS
L4 1 S L2 AND MEMOR?
L5 1 S L2 AND CONTROL?
L6 1 S L2 AND CLOCK?
L7 1 S L2 AND DATA?
L8 0 S L2 AND BUS?
L9 1 S L2 AND SYNCHRONOUS?
L10 1 S L2 AND PHAS?
L11 1 S L2 AND DELAY?
L12 0 S L2 AND ECHO?

Search Program

Case under review	Patent searched for	Noteable comment:
8,798,227	3,368,203	Checking system, delay line synchronization.
Class: 711 / 167		
8,798,227	3,377,621	Phase counters.
Class: 711 / 167		
8,798,227	3,417,378	Timing and control.
Class: 711 / 167		
8,798,227	3,493,936	Controller with memory and logic circuit, timing and delay.
Class: 711 / 167		
8,798,227	3,629,846	Time slot delay storage, multi-phase.
Class: 711 / 167		
8,798,227	4,270,185	Synchronizer for transmitter and receiver.
Class: 711 / 167		
8,798,227	4,288,860	FIFO Buffer, assynchronous clock, speed change.
Class: 711 / 167		
8,798,227	5,408,639	Multiple clocks system.
Class: 711 / 167		
8,798,227	5,522,067	Phased locked loop.
Class: 711 / 167		
8,798,227	5,652,733	Multiphase delayed clock.
Class: 711 / 167		
8,798,227	5,684,973	Multibank, delay line DRAM.
Class: 711 / 167		
8,798,227	5,699,548	Write through with synchronizer.
Class: 711 / 142		
8,798,227	5,737,748	Suspended clock.
Class: 711 / 142		
8,798,227	2,945,213	Delay means.
Class: 711 / 100		
8,798,227	2,993,195	Clock generator and delay.
Class: 711 / 100		
8,798,227	2,994,065	Synchronized storage.
Class: 711 / 100		
8,798,227	4,011,556	Command timing signals, pattern generation.
Class: 711 / 100		
8,798,227	4,376,974	Offset comparator.
Class: 711 / 100		
8,798,227	4,639,890	Phase matching to multiple sources.
Class: 711 / 100		
8,798,227	4,924,426	Create timing from sync signal.
Class: 711 / 100		